

HIGH PERFORMANCE Q-BAND 0.15 μ m InGaAs HEMT MMIC LNA

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Abstract

A monolithic three-stage pseudomorphic InGaAs HEMT low noise amplifier developed in our laboratory exhibits state-of-the-art low noise and gain performance at Q-band frequencies: it demonstrated 22 dB of gain with 3 dB noise figure from 41 to 45 GHz. From 35 to 50 GHz, it gave a flat gain response of over 22 dB gain across the Q-band range. This amplifier uses 0.15 μ m gate length GaAs-based pseudomorphic HEMTs with on-chip matching circuits and bias circuits. The chip size is 2.3 x 1.0 .mm²

Introduction

Significant progress has been made recently in HEMT technology to push the GaAs-based HEMTs into a wide range of system applications like millimeter-wave radar, satellite communication, electronic warfare, and surveillance system applications. Monolithic 20 and 44 GHz amplifiers are important building blocks for future EHF SATCOM applications with the advantages of high reliability, small size and weight, and low power consumption [1]. Previous reported 44 GHz LNAs have had noise figures of 4-6 dB with medium gain[2,3]. This work reports the development of a fully monolithic low noise amplifier (LNA) with on-chip matching and biasing circuits achieving a 3 dB noise figure with over 22 dB of gain across the Q-band range.

Material and Device

The GaAs-based pseudomorphic HEMT (pHEMT) structure was chosen for its low noise characteristics and mature fabrication technology. Figure 1 shows a cross section of the pHEMT device. The AlGaAs/InGaAs HEMT heterojunction was grown by MBE. The doping of the AlGaAs gate layer is sufficiently low for good Schottky gate characteristics. A planar-doped with Si atom at a sheet density of 5×10^{12} cm⁻² is employed to achieve good aspect ratio for high transconductance and good breakdown voltage [4,5]. A thin 90 \AA In_xGa_{1-x}As (x=0.25) layer is inserted between

AlGaAs spacer layer and GaAs buffer layer to form the channel for its superior electron transport properties (better channel confinement, higher electron mobility and saturation velocity). The 0.15 μ m T-shaped gate was patterned by a three- layer electron beam (E-beam) lithography process to minimize the gate resistance and the devices are passivated with silicon nitride for high reliability [6]. Typical DC transconductance of the devices is around 800 mS/mm.

A 75 μ m device size was selected for the Q-band LNA work because it provided a good impedance range for matching circuit design. The tested devices and passive elements were designed for on-wafer probing.

Device Characterization and Circuit Design

The objective was to design a 3.5 dB (max.) noise figure and 20 dB gain MMIC amplifier that covers 43 to 45 GHz frequency band. A three-stage circuit topology was chosen to achieve the targeted specifications. The amplifier was designed with broader bandwidth to enhance the circuit yield with the consideration of variations from the materials or processing.

Device equivalent circuit parameters were extracted from the measured S-parameters after removal of parasitics through a method of successive Z-to-Y and Y-to-Z transformations. This approach yields the accurate determination of all the parameters of an equivalent network model for the HEMT devices tested. Figure 2 shows the four measured S-parameters overlaying with the modeled results from 1 to 40 GHz. It fits very well across the whole range. Figure 3 displays the equivalent circuit model with the element values at low noise bias condition (10 mA). We also measured the devices at high gain conditions (ex. 18 mA) for the second and third stage device model. The 26 to 40 GHz noise parameters (F_{min}, G_{opt}, B_{opt}, and R_n) were measured on-wafer using a noise measurement test set from a modified ATN test system [7]. The minimum noise figure of tested devices measured at 40 GHz is 1.2 dB, which is consistent with other measurements at 18, 60, and 94 GHz [8].

These device models were then used to design the matching networks for the three-stage LNA. The input matching network was designed to give the best possible noise figure while maintaining a good associated gain. High impedance inductive transmission lines were added between the source of the HEMTs and the ground vias to improve the input match and for increased stability. The second and third stages matching circuits were designed to give the best gain and flatness while remaining unconditionally stable from DC to 60 GHz. The circuit schematic diagram is illustrated in Figure 4. The design used shorted stubs for the matching elements and on-chip bias networks consisting of thin-film resistors and MIM capacitors are used as DC blocks. There is a two-stage test cell shown in Figure 5 for diagnostic purposes.

A photo of the completed 3-stage LNA circuit is shown in the Figure 6. The chip dimensions are 2.3 x 1.0 mm².

Fabrication and Results

The MMIC was fabricated on 100 μ m thick GaAs substrate. A standard low noise pHEMT material structure was used (Figure 1). The 0.15 μ m gates were defined using E-beam lithography. This MMIC process included tantalum nitride thin film resistors, silicon nitride dielectric for MIM capacitors and device passivation, lift-off air-bridge, and via holes were fabricated using reactive ion etching.

The 44 GHz LNA circuits were tested on wafer from 35 to 50 GHz. Figure 7 illustrates the performance with the bias of the first stage adjusted to give the best noise figure, the second and third stages biased to give best gain response. The LNA gives a flat gain response of over 22 dB from 35 to 50 GHz. The S₁₁ is -7 dB and S₂₂ is -10 dB at 44 GHz. Several chips were mounted on the WR22 waveguide test fixtures (stepped-ridge waveguide to microstrip transitions) to test gain, noise, and power performance as shown in the Figure 8. Figure 9 shows the gain and noise performance as compared with modeled data. The gain is 21.5 ± 1 dB from 36 to 46 GHz with an average noise figure of 3 dB. At 40 GHz, the noise figure is 2.8 dB. The typical 1dB compression point of the 3-stage LNA is around +11 dBm measured at 44 GHz.

Conclusion

We have achieved state-of-the-art low noise and gain performance on the first design iteration. The excellent noise and gain performance of the amplifier can be attributed to careful measurement, accurate modeling, thorough design, and repeatable fabrication. This Q-band MMIC LNA with gain of over 20 dB and a noise figure less than 3.5 dB from 36 to 46 GHz can be used as the front end of a EHF receiving system. It

can also be used as a gain block amplifier due to the flat gain response and high 1 dB compression point. InGaAs pHEMTs provide superior performance margin over conventional AlGaAs/GaAs HEMTs or MESFETs. The pHEMT technology is mature and very attractive for the array applications. It can integrate LNAs, phase shifters, driver amplifiers, and power amplifiers for light weight, high reliability, low cost and mass production.

Acknowledgment

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Layer	Thickness	Alloy Composition	Doping
Cap	350Å	GaAs	$n=4 \times 10^{18} \text{ cm}^{-3}$
Gate	400Å	$\text{Al}_{0.24}\text{Ga}_{0.76}\text{As}$	$n=7 \times 10^{17} \text{ cm}^{-3}$
Spacer	45Å	$\text{Al}_{0.24}\text{Ga}_{0.76}\text{As}$	undoped
Channel	90Å	$\text{In}_{0.25}\text{Ga}_{0.75}\text{As}$	undoped
Buffer	1μm	GaAs	undoped
Substrate	635μm	GaAs	$\text{SI } <100>$

Fig. 1 Cross-section of the AlGaAs/InGaAs/GaAs pHEMT.

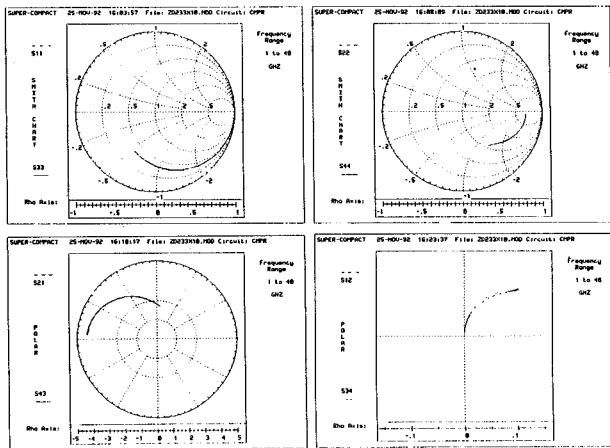


Fig. 2 0.5-40 GHz S parameters of $0.15 \times 75 \mu\text{m}$ pHEMT. S₁₁, S₂₂, S₂₁, and S₁₂ are modeled data and S₃₃, S₄₄, S₄₃, and S₃₄ are measured data.

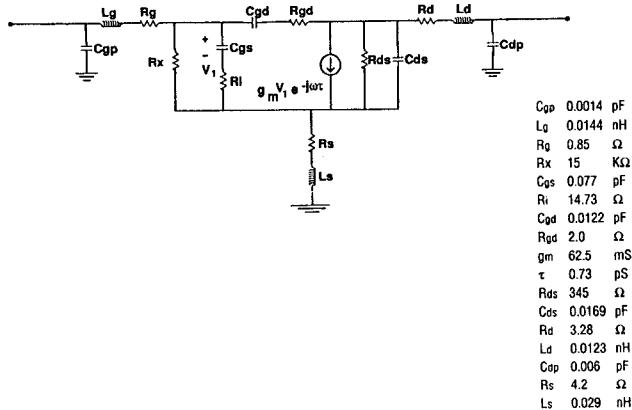


Fig. 3 75 μm low noise pHEMT model.

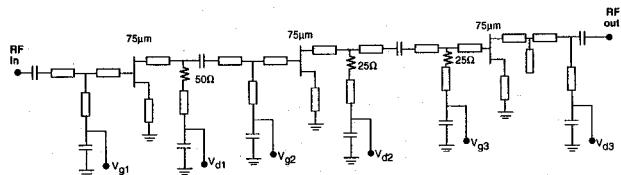


Fig. 4 Q-band 3-stage LNA circuit schematic diagram.

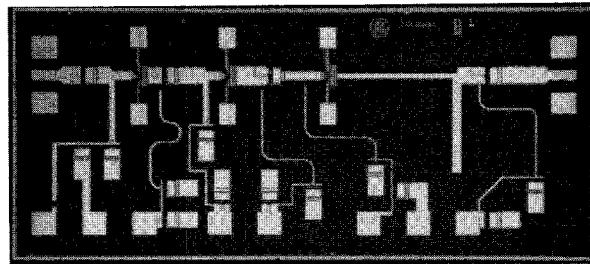


Fig. 5 Completed Q-band 3-stage MMIC LNA.

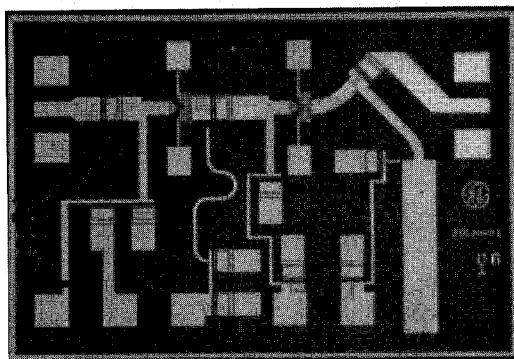


Fig. 6 Completed Q-band 2-stage MMIC LNA.

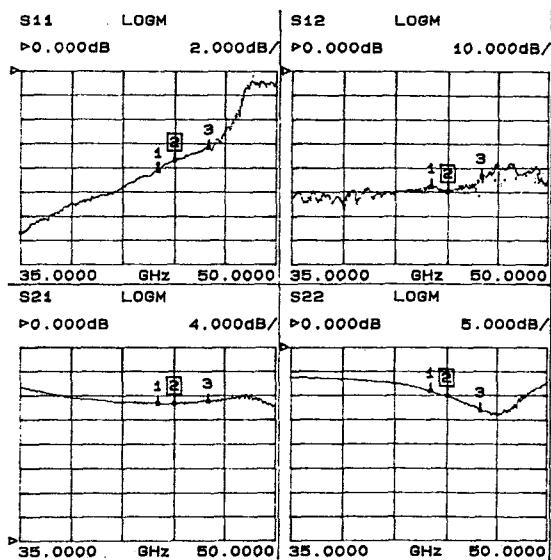


Fig. 7 On-wafer measured performance of Q-band 3-stage LNA from 35 to 50 GHz.

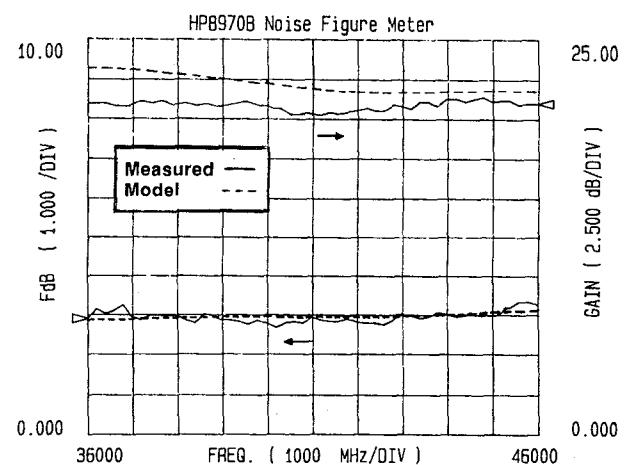


Fig. 9 Q-band 3-stage MMIC LNA measured gain and noise performance compared with modeled results from 36 to 46 GHz.

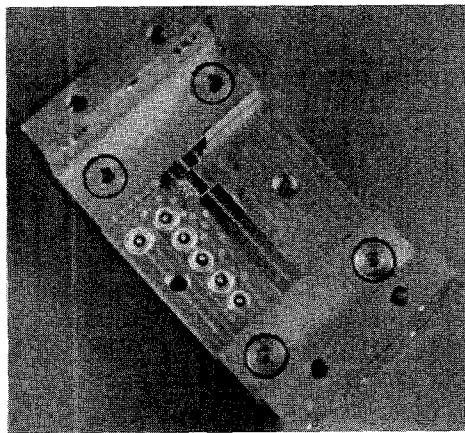


Fig. 8 A Q-band 3-stage MMIC LNA mounted in waveguide test housing.